CLAIMS

1. A magnetic memory cell comprising:

a magnetic storage element, the magnetic storage element having a plurality of layers including a first magnetoresistive layer and a second magneto resistive layer and a non-magnetic material layer therebetween;

a current control element coupled to the magnetic storage element to control current flow therethrough, the current control element including a first region of material of a first conductive type and a second region of material of a second conductive type and defining a junction therebetween, wherein the junction extends transversely to each of the layers in the magnetic storage element.

2. The magnetic memory cell of claim 1 wherein the first region of the current control element is in the form of a core and the second region is in the form of a circumferential layer formed on the core, wherein the first and second regions form a pillar structure.

3. The magnetic memory cell as claimed in claim 2 wherein the magnetic storage element is connected to the core at one end of the pillar structure.

4. The magnetic memory cell of claim 1 wherein the current control element comprises a diode.

5. The magnetic memory cell of claim 1 wherein the first region comprises silicon and the second region comprises a metal silicide such that the junction between the first region and the second region forms a pn junction of a diode.

6. The magnetic memory cell of claim 2 wherein the first region is in the form of a silicon core and the second region is in the form of a circumferential layer of metal silicide formed on the core, the junction between the first and second regions comprising a pn junction of a Schottky diode.

7. The magnetic memory cell of claim 6 wherein the second region is platinum silicide.

8. The magnetic memory cell of claim 2 wherein the pillar structure is disposed within a first conductor line such that the first conductor line surrounds the sides of the pillar structure.

9. The magnetic memory cell of claim 1 wherein the magnetic storage element and the current control element are integrated.

10. A cross point resistive memory device comprising:

a first array of memory cells arranged generally in a plane, each of the memory cells including a memory storage element having a diode coupled thereto to control current through the memory storage element, wherein the diode includes a first region of material of a first conducting type and a second region of material of a second conducting type and defining a junction therebetween, wherein the junction extends transversely to the plane of the array of memory cells, the memory device being operable to pass current through a selected one of the memory storage elements with the coupled diode junction forward conducting.

11. The memory device of claim 10 wherein the first region of the diode is in the form of a core and the second region is in the form of a circumferential layer about the core such that the first and second regions define a pillar structure.

12. The memory device of claim 10 wherein the memory storage element and the diode are integrated.

13. The memory device of claim 10 wherein the diode comprises a Schottky diode.

14. The memory device of claim 11 wherein the memory storage element is connected to the core at one end of the pillar structure.

15. The memory device as claimed in claim 11 wherein the first region is silicon and the second region is a metal silicide such that the junction between the first and second regions comprises a pn junction of a Schottky diode.

16. The memory device of claim 15 wherein the second region comprises platinum silicide.

17. The memory device of claim 11 wherein the pillar structure is disposed within a first conductor line such that the first conductor line surrounds sides of the pillar structure.

18. The memory device of claim 17 wherein there are a plurality of such first conductor lines whereby the array of memory cells comprises rows and columns of memory cells with each column of cells being connected to a common one of said first conductor lines.

19. The memory device of claim 18 wherein there is a plurality of second conductor lines and each row of cells is connected to a common one of said plurality of second conductor lines whereby the plurality of second conductor lines extends generally transversely to the first conductor lines.

20. The memory device of claim 19 further providing a plurality of such arrays of memory cells, with the arrays being disposed in a layered arrangement.

21. The memory device of claim 9 wherein the memory cells are magnetoresistive random access memory cells.

22. A method of constructing the memory cell of claim 10 comprising:

constructing a silicon column and depositing a metal thereon to form a metal silicide as a circumferential layer on a core of silicon, thereby forming a pillar diode.

23. The method of constructing the memory cell as claimed in claim 22 wherein the silicon column is constructed from amorphous silicon.

24. The method of constructing the magnetic storage cell of claim 1 wherein an array of such current control elements is initially constructed whereafter the layers of the magnetic storage element are deposited in order to construct an array of memory cells in which the magnetic storage elements and the current control elements are integral.

25. The method of claim 22 further comprising providing a first conductor line to surround the pillar diode.

26. The method of claim 25 further providing isolation material wherein the isolation material defines a trench surrounding the pillar, the method further comprising filling the trench with conductor material to form the first conductor line.